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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/792,006	03/03/2004	Chung-Hui Chen	TSMC2003-0803(N1280-00040	4259

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EXAMINER	
COX, CASSANDRA F	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/792,006	CHEN, CHUNG-HUI	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-11 and 18-20* is/are allowed.

6)☒ Claim(s) *1,3,12,14,16 and 17* is/are rejected.

7)☒ Claim(s) *2,4-6,13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 16 recites the limitation "the voltage comparator" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 17 recites the limitation "the lock signal" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 12, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Beling et al. (U.S. Patent No. 4,272,712).

In reference to claim 1, Beling discloses in Figure 1 a clock lock detection circuit comprising: a first input indicating an edge of a first clock (output of pulse shaper 10); a second input indicating a corresponding edge of a second clock (output of divider 14)

wherein the second clock is expected to be synchronized with the first clock with an allowable time difference; a difference generation module (12) for generating a difference signal based on the time difference between the first and second inputs; and a voltage divider (24, 26) for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs. The same applies to claim 12.

In reference to claim 3, Beling discloses in Figure 1 that the difference generation module is a phase comparator, it is considered to be well known to one skilled in the art that phase comparators can be constructed as XOR gates, of which fact official notice is taken. The same applies to claim 14.

7. Claims 1, 3, 12, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Shibano (U.S. Patent No. 4,613,799).

In reference to claim 1, Shibano discloses in Figure 8 a clock lock detection circuit comprising: a first input indicating an edge of a first clock (S2); a second input indicating a corresponding edge of a second clock (S1) wherein the second clock is expected to be synchronized with the first clock (S2) with an allowable time difference; a difference generation module (65) for generating a difference signal based on the time difference between the first and second inputs; and a voltage divider (74) for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs. The same applies to claim 12.

In reference to claim 3, Shibano discloses in Figure 8 that the difference generation module (65) is a phase comparator, he further discloses in Figure 3 an alternative method of implementing a phase comparator (7) that is an XOR gate, see column 6, lines 51-53. The same applies to claim 14.

8. Claims 1, 3, 12, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Meyer et al. (U.S. Patent No. 5,889,439).

In reference to claim 1, Meyer discloses in Figure 1 a clock lock detection circuit comprising: a first input indicating an edge of a first clock (2); a second input indicating a corresponding edge of a second clock (3) wherein the second clock is expected to be synchronized with the first clock with an allowable time difference; a difference generation module (1) for generating a difference signal based on the time difference between the first and second inputs; and a voltage divider (9) for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs. The same applies to claim 12.

In reference to claim 3, Meyer discloses in Figure 1 that the difference generation module (1) is a phase detector, it is considered to be well known to one skilled in the art that phase detectors can be constructed as XOR gates, of which fact official notice is taken. The same applies to claim 14.

Allowable Subject Matter

9. Claims 7-11 and 18-20 are allowed.

10. Claims 2, 4-6, 13, and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 16-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: Claims 2 and 13 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the voltage divider module (206, 212) has a CMOS inverter (206) and a capacitor (212) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 4-6 and 15-17 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit further comprises a voltage comparator (214) for comparing the indication voltage against a predetermined threshold voltage for generating a lock signal in combination with the rest of the limitations of the base claims and any intervening claims.

13. The following is an examiner's statement of reasons for allowance: Claims 7-11 and 18-20 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit includes a voltage divider module (206, 212) containing a capacitor (212) for receiving the difference signal and generating an indication voltage which varies due to a charging and discharging process (performed by inverter 206) of the capacitor (212); and a voltage comparator (214) for comparing

the indication voltage against a threshold voltage in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC
CC
April 1, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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